PF32 USER MANUAL

v1.5.14

WARRANTY AND DISCLAIMERS

Use of this product and the associated software implies acceptance of the Photon Force terms of use.

Bare electronic components are susceptible to electrostatic discharge (ESD). Failure to employ good practice in handling the hardware, or to observe and comply with the warnings and handling precautions stated in this guide will void product warranty.

This product may not be used in military, aerospace, medical or other safety critical applications without the express written permission of Photon Force Ltd. Any such use is undertaken entirely at the customer's own risk.

Specifications are subject to change without notice.

PHOTON FORCE

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WARNINGS

- Store the camera at temperatures between 0 and 40°C
- Avoid humid environments (70% and above)
- Keep out of direct sunlight and away from heaters
- Avoid vibrating surfaces when mounting the PF32 system
- Avoid areas that contain dust/particulates

PACKAGE CONTENTS

Upon receiving your PF32 camera, please check the contents:

PF32 Camera

5V DC power supply

USB3 cable

INTRODUCTION

The PF32 system consists of 1024 single-photon avalanche diodes (SPADs) arranged in a 32 × 32 array. Each pixel has its own photon counting and timing electronics, making it a powerful and unique single-photon sensitive time-resolved imager. It can be used in time-correlated single-photon counting (TCSPC) mode with a photon timing accuracy of 55 ps, or it can be used in photon counting mode as a single-photon sensitive high frame rate camera. In TCSPC mode, the sensor can be operated in conjunction with a wide variety of light sources, such as pulsed lasers and LEDs, to perform time-resolved measurements. To accommodate the differing properties of these devices, a number of clocking/synchronisation options can be provided.

The camera has a CS-mount thread enabling the use of a wide variety of lenses, and with the addition of adapters this can be extended to almost any lens the user wishes to employ. It is easily connected to a computer through a USB 3.0 connection, and requires a simple 5V supply for the entire system.

FEATURES AT A GLANCE:

- 32×32 pixel TCSPC imaging array.
    - Fully digital photon counting and time-stamping (no analogue readout noise).
    - In-pixel dual mode electronics:
        - 55ps resolution 10-bit Time to Digital Converter (TDC) time-stamping (1,023 time bins).
        - 7-bit photon counting (count up to 127 photons per pixel per frame)
    - Pipelined operation: simultaneous data acquisition and readout.
- Flexible readout timing allows an increased frame rate for a subset of pixels or reduced number of counter/TDC bits (LSB first).
- Row and column enable/disable settings to define region of interest.
- Optional calibration mode to lock TDC resolution to laser or reference frequency.
- External laser synchronisation signal and reference clock inputs to provide TDC stop signal and calibration loop reference frequency.
- Individual power and bias supplies for noise-sensitive features.

PF32 GENERAL CHARACTERISTICS

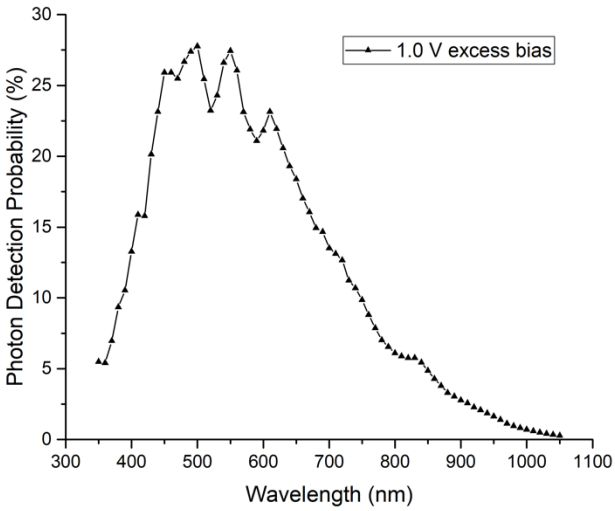
Within each pixel of the PF32 sensor, the detection of single photons is performed by the SPAD active area. This active area is surrounded by the necessary electronics to bias and quench the SPAD, as well to time and count the detected photons. In a traditional TCSPC setup, each detector would need its own external electronics to time-tag the photon's arrival, whereas the PF32 is intended to provide a compact and highly parallel means of data acquisition for a variety of applications such as fluorescence lifetime imaging microscopy (FLIM) and 3D active imaging.

The active area is a silicon p-n junction which is reverse-biased beyond its breakdown voltage in the so-called "Geiger-mode". In this regime, the absorption of a single photon gives rise to a detectable current pulse due to impact ionisation events within the semiconductor lattice enabled by the acceleration of the initial photo-generated carriers in the high electric field. After the onset of an avalanche, the SPAD is disarmed by reducing the bias to a value below the breakdown voltage. The SPAD is then re-armed after a short period known as the "dead time". The dead time (sometimes called the "hold-off" time) is needed to ensure that any carriers trapped within the semiconductor structure following an avalanche event are released; if the dead time is too short and the SPAD is re-armed, any remaining trapped carriers may trigger another avalanche, referred to as an "afterpulse". Afterpulsing effectively increases the dark count rate (DCR) of the SPAD, thus decreasing the signal to noise ratio (SNR). For this reason, the dead time is set to a sufficiently long period to negate the deleterious effects of afterpulsing.

The DCR itself is a function of temperature and bias voltage; increasing either, or both, of these parameters also increases the DCR. The final contribution to the DCR is through cross-talk, whereby during the avalanche process some photons are emitted during the large flow of high-energy carriers. Due to the large distance between active areas, the contribution of cross-talk is negligible.

The photon-detection efficiency is also a function of bias voltage as shown in the figure below.

The final important figure of merit is the jitter, or instrument response function (IRF), which relates to the uncertainty in absolute timing of the stochastic avalanche process in response to the detection of a photon. The IRF of the SPADs within the PF32 array is ~150 ps.



Photon detection probability vs. wavelength of a PF32 pixel.

Further reading is available here:

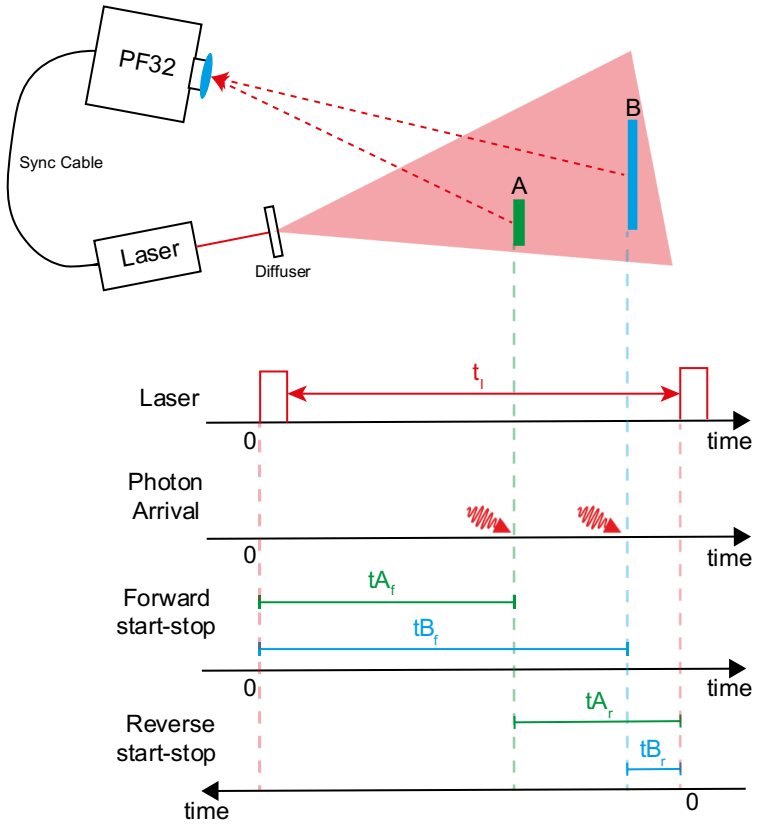
- Paper describing the SPAD device: *J. A. Richardson, L. A. Grant and R. K. Henderson; "Low Dark Count Single-Photon Avalanche Diode Structure Compatible With Standard Nanometer Scale CMOS Technology", Photonics Technology Letters, IEEE, Jul. 2009, vol. 21, no. 14, pp. 1020-1022.*

- Paper describing the PF32 device: *J. Richardson, R. Walker, L. Grant, D. Stoppa, F. Borghetti, E. Charbon, M. Gersbach and R. K. Henderson; "A 32×32 50ps resolution 10 bit time to digital converter array in 130nm CMOS for time correlated imaging", IEEE Custom Integrated Circuits Conference (CICC), San Jose, USA, September 2009, pp. 77-80.*

PF32 MODES OF OPERATION

TCSPC MODE

Often, TCSPC is thought of as a fast stopwatch – the start being the emission of the pulsed light source and the stop being the detection of a single photon. However, like many TCSPC systems, the PF32 performs reverse start-stop measurements: the detection of a single photon starts the time-to-digital converter (TDC) and the next synchronisation pulse stops this process. This is explained in the following diagram.

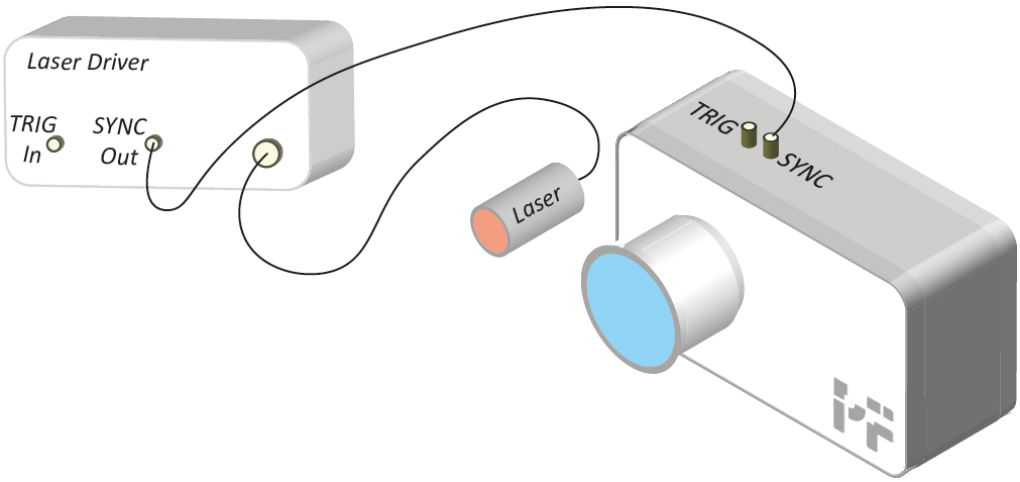


Using a basic laser-ranging setup as an example, the reverse start-stop principle can be explained. A pulsed laser beam passes through a diffuser and illuminates 2 surfaces, A and B. Photons are scattered from these surfaces and some will be collected by the PF32. Below the ranging setup we show the timing of the processes involved (for simplicity, we consider a half round trip). The laser period is t_l, and at some time later, photons are detected by the PF32. Considering forward start-stop, the time stamp given to a photon from surface A (tA_f) has a lower value than that of a photon from surface B (tB_f). In reverse start-stop, the detection of a photon starts the timing process and the timing information is given relative to the subsequent laser sync pulse. This results in the time stamp for surface A (tA_r) being of a greater value than that of surface B (tB_r).

Reverse start-stop measurements are advantageous since they ensure that the counting electronics are only active when a photon has been detected; in forward start-stop, the synchronisation signal starts the timing and the detection of a photon stops the timing. This means that the timing electronics are in constant use and need to be reset every synchronisation period, potentially increasing readout dead time, power consumption, and heat dissipated through the device.

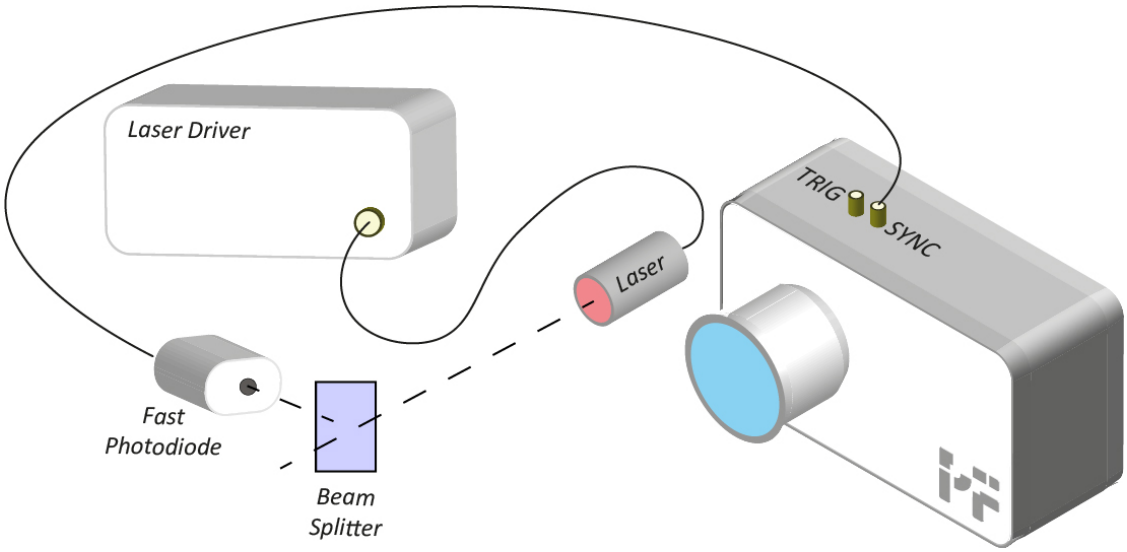
The PF32 can accept a synchronisation signal via the Sync SMA connector (3.3V max as set out in the synchronization document) in laser-is-master mode. Alternatively, the FPGA within the camera can be used to provide the synchronisation signal to the TDC and also output this to the light source via the TRIG SMA connection (0 to 3.3V).

The image below demonstrates the basic setup in the laser-is-master mode:



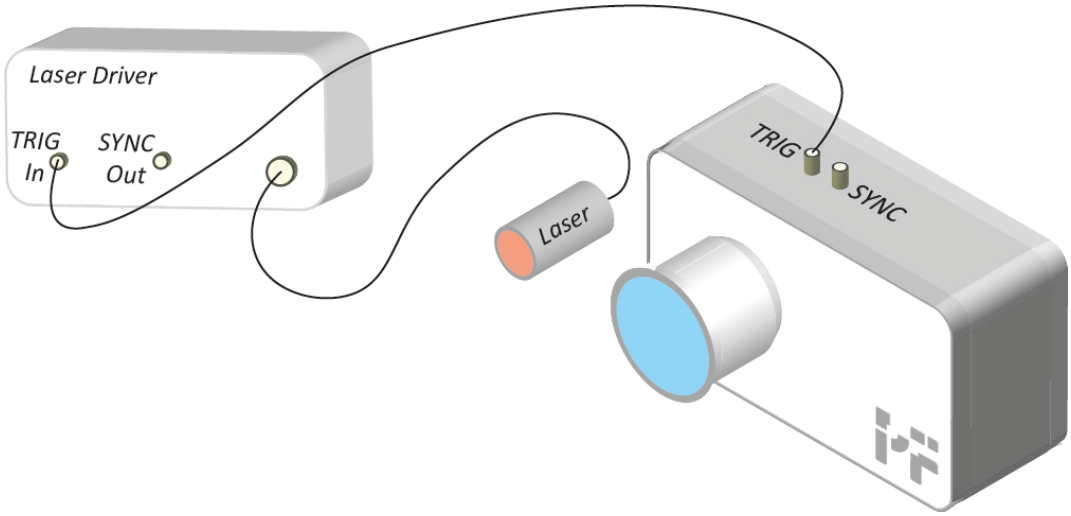
Here, the laser driver is the master clock for the TCSPC measurement: it provides the timing for both the laser to fire and for the stop signal for the camera through the sync input SMA of the PF32.

If the laser being used does not have a synchronisation output, a beam-splitter can be used to take a small portion of the outgoing power and direct it onto a fast photodiode. The output of the photodiode can then be used as the sync pulse as shown below.



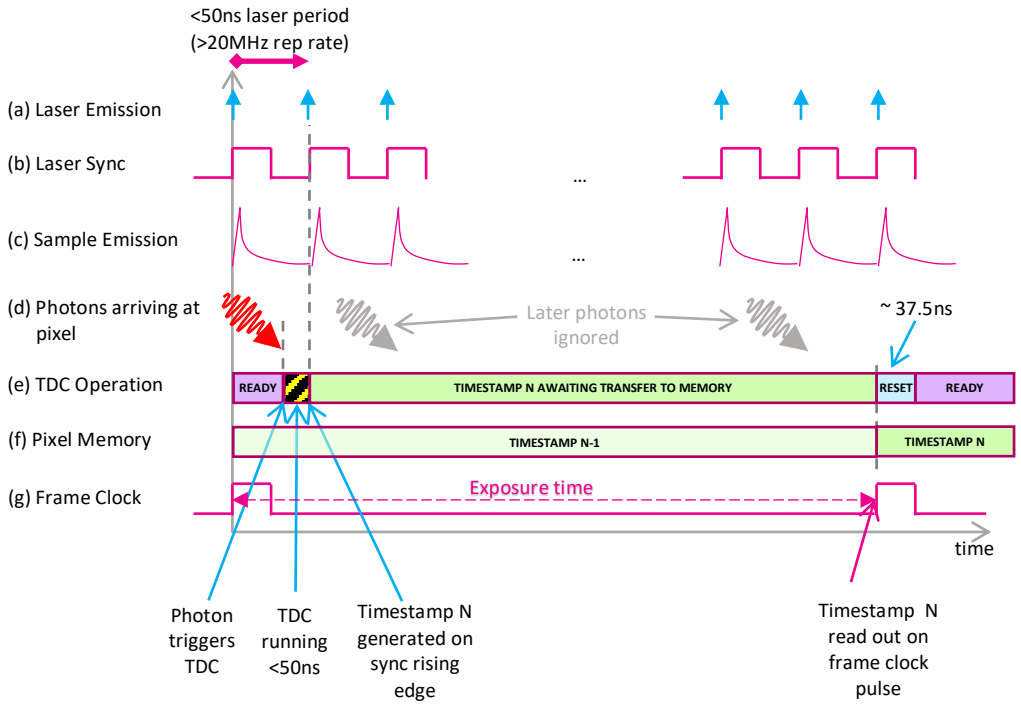
If the laser driver does not have a synchronization output, the master clock for the TCSPC measurement can be provided by taking part of the outgoing light and directing it onto a fast photodiode.

If, however, you'd like to use the internal clock from the PF32 to trigger your laser, the following configuration can be used.



If the pulsed light source accepts a trigger, the PF32 can be used as the master clock via the TRIG output (3.3V)

The following diagram shows the intended method of operation of the PF32's TCSPC mode as detailed in the figure caption.



Timing diagram showing intended TCSPC use: In this example, (a) a laser firing at 20MHz is directed at a sample that absorbs the laser light and re-emits at a longer wavelength due to photoluminescence with a temporal decay as shown in (c). Here we examine the timing of a single PF32 pixel where the TDC is in the ready state (e) until a photon is detected from the sample (d). The TDC starts to run and is stopped by the following laser sync pulse (b). This time stamp (f) is then awaiting transfer to memory until the start of the next frame, during which time the TDC cannot register any other photon arrivals. The frame clock (g), or exposure time, therefore dictates the highest count rate achievable by any single pixel within the PF32 array since each TDC can only generate one timestamp per frame.

While there are benefits of reverse start-stop TCSPC measurements, some care does need to be taken in order to extract the best performance from the system. Since the TDC provides 1,023 time bins (10 bit) with ~55ps resolution, the maximum unambiguous measurement is

approximately 56.3ns. If longer intervals are measured, the time-stamp value will 'wrap around', such that a 57.3ns interval is indistinguishable from 1ns. However, it should be noted that the measurement uncertainty (jitter) accumulates over time; the more times the TDC wraps around, the higher the jitter degradation. Care should therefore be taken to provide a maximum STOP waveform period of under 56.3ns. This can be accomplished by delaying the synchronisation pulse with an active delay generator, or passively with lengths of coax cable.

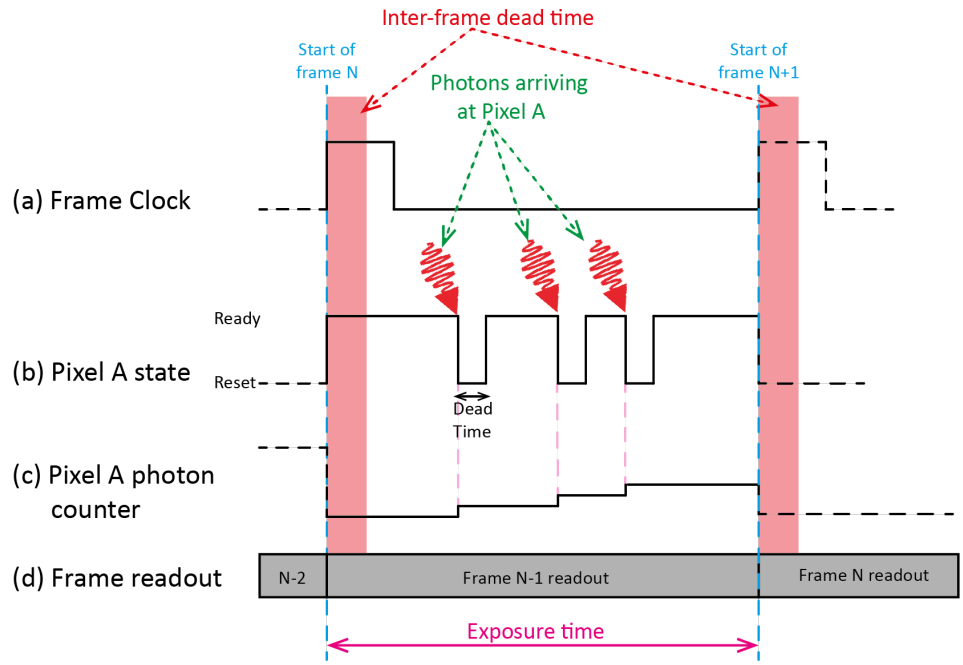
If no photon is detected within the frame time, a count is added to the zero time bin.

As with all TCSPC systems, care should be taken to avoid the effects of pulse pileup, which will distort the photon-counting histogram. It is essential that the photon counting rate per pixel is less than 10% of the sync frequency in order to avoid pulse pileup effects.

In both modes, an in-pixel memory stores the data captured during each frame time. This data is then read out during the following frame, while the pixel acquires new data.

PHOTON COUNTING MODE

In photon counting mode, the TDC is configured to simply count the number of photons received during each frame time. No sync is required for the measurement process, making photon counting mode a useful tool for initial setup/alignment of the system before taking TCSPC data. In this mode, each pixel can count multiple photons per frame as shown below.



In photon counting mode, the frame clock (a) dictates the maximum frame rate (a single pixel has been shown for clarity). At the start of each frame there is a short deadtime (shown in red) of ~50ns before which detected photons will not be counted, after which each pixel can count multiple photons within a frame (7 bit counter, therefore 127 photons per frame). After the detection of a photon (b), the counter increments (c) and the SPAD is reset. During the reset process the SPAD is off for ~50ns. This process is repeated until the end of the frame when the next frame clock pulse initiates the transfer of the data to the readout stage (d). It should be noted that the 7 bit counter will reset to zero after 127 detection events. A sufficiently short frame time should be chosen to ensure that wrap around does not occur. The camera's 'frames to add' setting allows multiple frames to be summed digitally to achieve a larger maximum count value if needed.

PF32 ELECTRICAL CONNECTIONS

As shown in the figure above, at the top of the camera housing, there are 5 input and 2 output SMA connectors, the USB 3.0 connector and 5 V power supply terminal are located on the side of the housing. The table below describes the SMA connector functions:

Name	Voltage Range (V)	Description
FRM	0 to 5	Frame sync input for use with scanning systems
LINE	0 to 5	Line sync input for use with scanning systems
PIXEL	0 to 5	Pixel sync input for use with scanning systems
BLK	0 to 5	Blanking input for use with scanning systems
SYNC	0 to 3.3	External laser sync input signal
TRIG	0 to 3.3	External laser source trigger signal (output)
SHUT	0 to 3.3	Shutter output signal

TECHNICAL SPECIFICATIONS

Sensor Dimensions

Array size	32 × 32 pixels
	1.6 × 1.6mm
SPAD active area	6.95µm ⌀
Pixel pitch	50µm
Optical fill factor	1.5%

Optical / Electrical Performance

Photodetection efficiency	Peak 28% at 500nm
Dark noise:	<100Hz for 80% of pixels
Afterpulsing	<0.02%
Optical/Electrical Crosstalk:	None
Timing jitter:	<200ps FWHM

Photon Counting Mode

Photon counting:	7 bit in-pixel 16 bit in firmware
Maximum photon counting rate per pixel:	50MHz

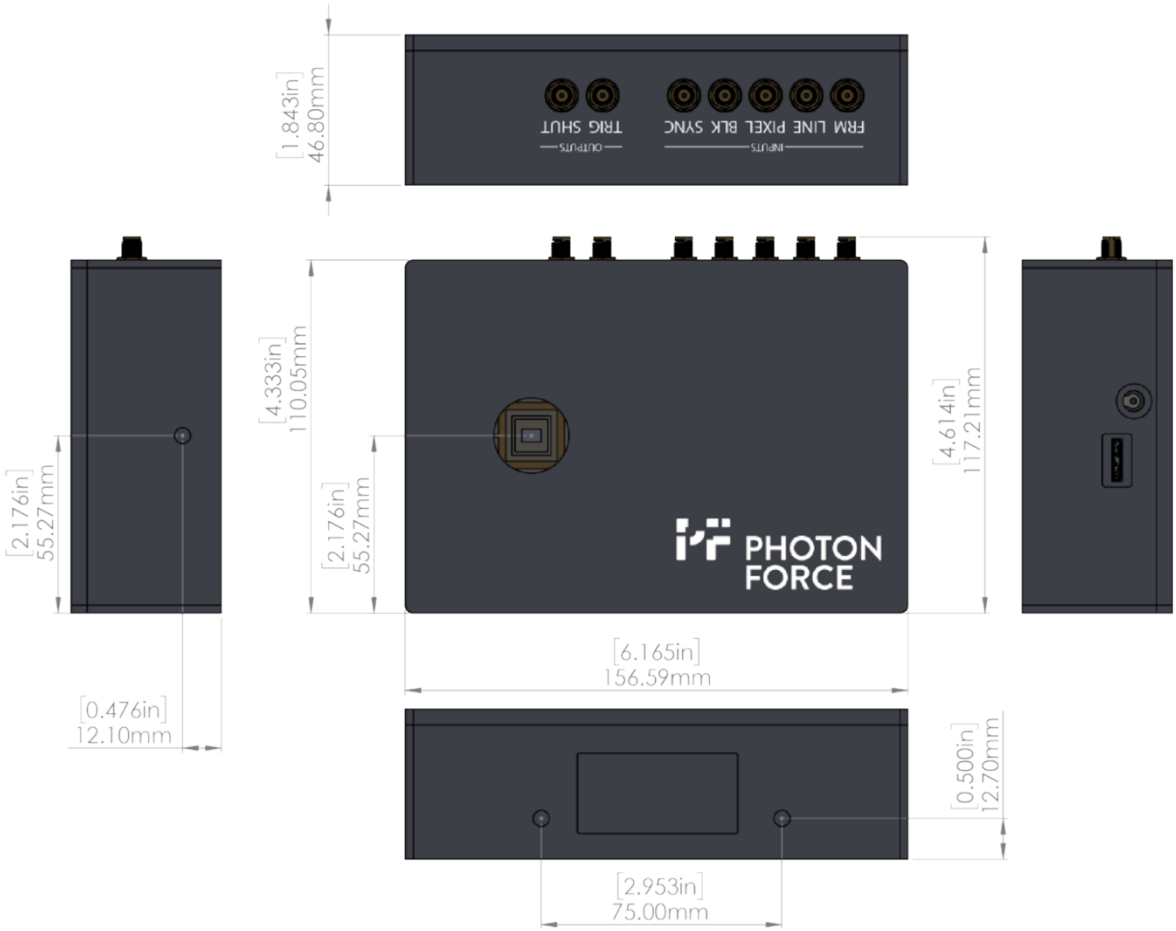
Time Correlated Mode

Temporal bin size:	55ps
Temporal range:	55ps - 57ns
TDC resolution:	10 bit
Maximum laser sync frequency (input or output):	100MHz
Laser sync input amplitude	3.3V
Laser sync output amplitude	3.3V

Readout & Control

Maximum sensor to firmware frame rate, 10-bit data	0.5Mfps - 8Mfps [1]
Raw data streaming frame rate to PC	300kfps (8 bit data) 150kfps (16 bit data) Higher frame rates may be achieved with ROI and/or lower bit-depth data. Please contact us for more details.
Inter-frame dead time	<50ns
X/Y Scanner synchronisation input signals	Pixel, line and frame clock
Exposure synchronisation signals	Blanking (3.3V / 5V input) Shutter (3.3V output)

MECHANICAL DRAWING



Dimensions in mm and [inches]

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